AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-22 (cancelled)

23. (currently amended) A semiconductor device comprising:

a plurality of first and second word lines;

a first bit line pair including a first bit line and a second bit line;

a second bit line pair including a third bit line and a fourth bit line;

a plurality of first DRAM memory cells provided at an intersection of said first word lines and said first bit line;

a plurality of second DRAM memory cells provided at an intersection of said second word lines and said second bit line;

a first MOSFET having a source and drain path coupled to said first bit line and said ~~second~~ third bit line;

a second MOSFET having a source and drain path coupled to said second bit line and said ~~third~~ fourth bit line;

a sense amplifier coupled to said third and fourth bit lines;

a first control line coupled to a gate of said first MOSFET; and

a second control line coupled to a gate of said second MOSFET,

wherein during a rewriting operation one of said first and second MOSFETs is in on-state and the other of said first and second MOSFETs is in off-state.

24. (original) The semiconductor device according to claim 23,

wherein during said rewriting operation said first and second control lines are set on different levels and said sense amplifier is used for rewriting to one of said first and second DRAM memory cells which is coupled to a selected word line of said plurality of first and second word lines, and

wherein said levels of said first and second control lines depend on a selection of said plurality of first and second word lines.

25. (original) The semiconductor device according to claim 24, further comprising:

a third bit line pair including a fifth bit line and a sixth bit line;

a third MOSFET having a source and drain path coupled to said third bit line and said fifth bit line; and

a fourth MOSFET having a source and drain path coupled to said fourth bit line and said sixth bit line,

wherein said first and second MOSFETs each have a thicker gate insulating layer than said third MOSFET.

26. (original) The semiconductor device according to claim 25,

wherein said third bit line pair is a global bit line pair for write operation.

27. (original) The semiconductor device according to claim 26, further comprising:

a fourth bit line pair including a seventh bit line and an eighth bit line;

a fifth MOSFET having a source and drain path coupled to said third bit line and said seventh bit line; and

a sixth MOSFET having a source and drain path coupled to said fourth bit line and said eighth bit line,

wherein said fourth bit line pair is a global bit line pair for read operation.

28. (original) The semiconductor device according to claim 27,

wherein after a first time period said levels of said first and second control lines are set on a same level.